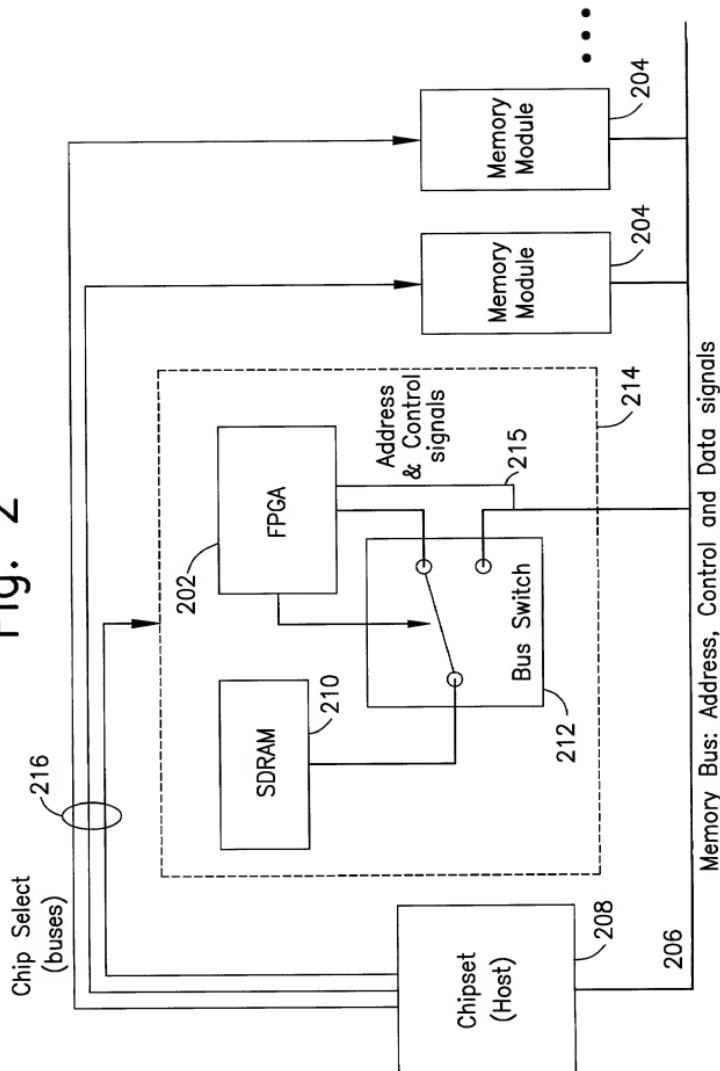


Fig. 1
Prior Art

Fig. 2



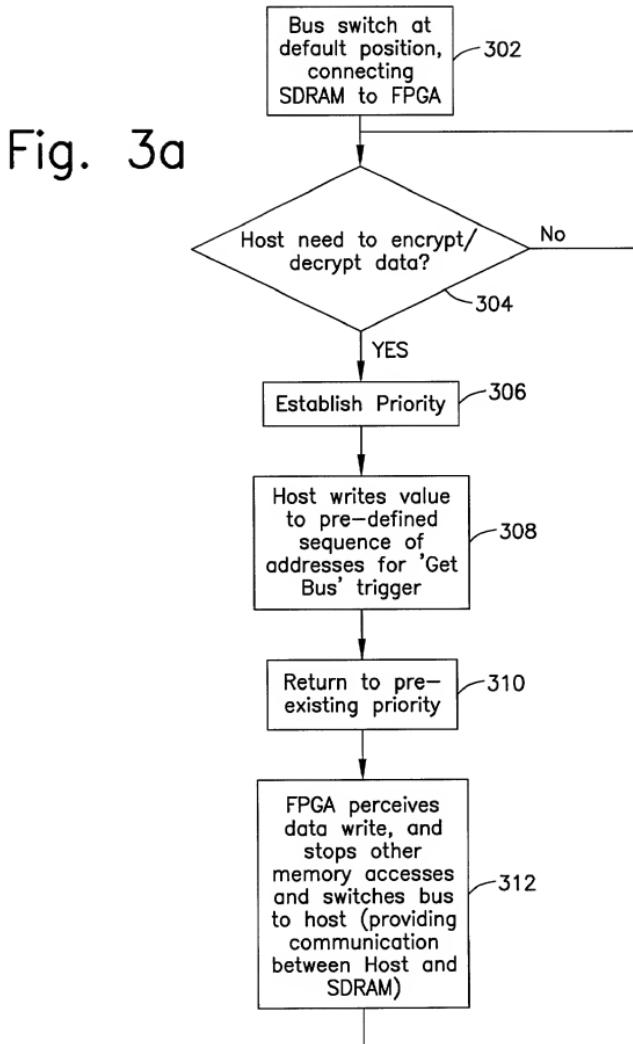
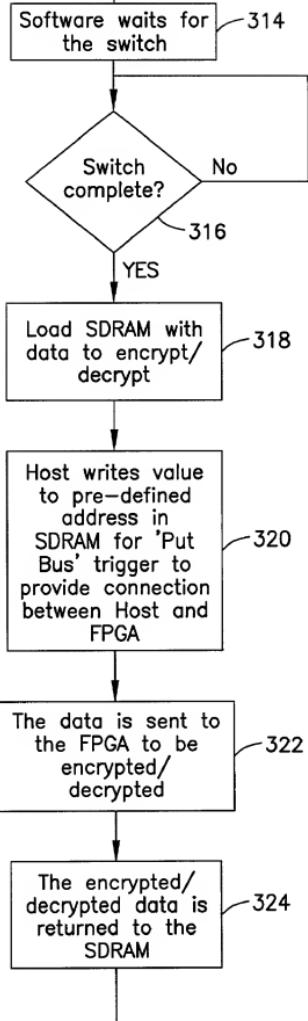


Fig. 3b

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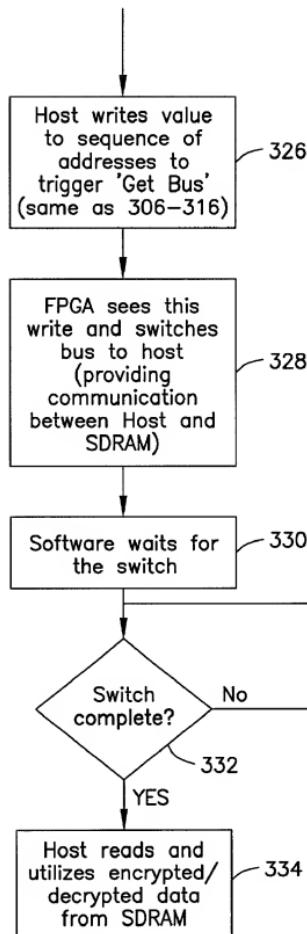


Fig. 3c

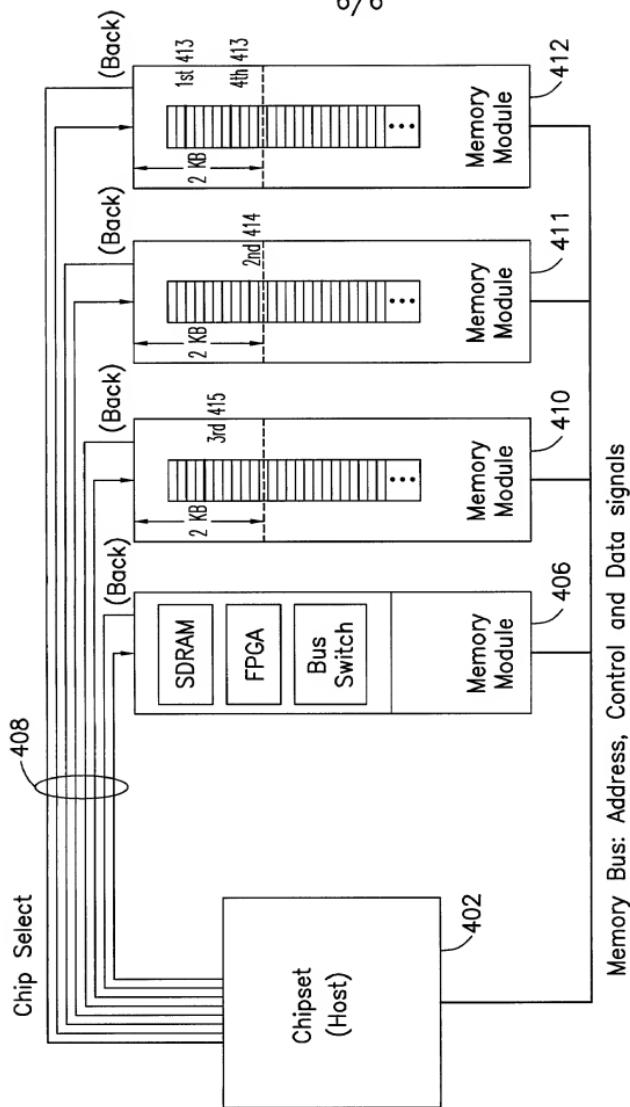


Fig. 4

Memory Bus: Address, Control and Data signals